

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 - 4 (CANCELLED).

5. (CURRENTLY AMENDED) A tailored integrated circuit interconnect module for reducing interconnections between fully tested integrated circuit chips comprising a support substrate having mounted thereon at least one primary integrated circuit device chip and a plurality of interacting peripheral integrated chip devices, said interconnect module including a plurality of interface pins, each integrated circuit device having a plurality of interface ports, at least one of which is connected to another one of said plurality of integrated circuit devices, at least one of said integrated circuit devices having an interface port connected to an interface pin whereby the majority of nodes on said peripheral devices are adapted to interface with nodes of said at least one or more primary IC devices integrated chip device in such a way as to condense the number of nets so that the total number of nodes connected to external pins is minimized.

6. (CURRENTLY AMENDED) The tailored integrated circuit interconnect module defined in claim 5 wherein said primary

integrated circuit ~~device-chip~~ chip device is a network processor and at least one of said other devices is a memory device.

7. (CURRENTLY AMENDED) The tailored integrated ~~circuit~~ interconnect module device defined in claim 5 wherein the interconnections between said devices have different impedances.